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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,896	07/28/2003	Chao-Wu Chen	M-15049 US	7428

7590 06/21/2005

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EXAMINER	
TRAN, MICHAEL THANH	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/628,896	CHEN ET AL.
	Examiner	Art Unit
	Michael t. Tran	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 28, 2003 through July 12, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,9,10,16 and 18* is/are rejected.

7)☒ Claim(s) *2-6,8,11-15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

MICHAEL TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated July 28, 2003 through July 12, 2004, claims 1-18 are active in this application.

Claim Objections

2. Claims 2-6, 8, 11-15, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1, 7, and 9 are rejected under 35 U.S.C 102(b) as being anticipated by

Tsang [U.S. Patent #4,376,300].

With respect to claim 1, Tsang discloses, in figure 1, a memory circuit comprising: an output data bus [26]; a memory array [18] receiving a memory address and providing output data from a memory access using the memory address, the memory array comprising a plurality of memory blocks [memory has a plurality of cells], and a control circuit [columns 5 and 6 state that there exist timing signals within the memory arrays; hence, it is reasonable to infer that there exist an element to handle the timing signals within the arrays] providing a timing signal that is asserted at a first predetermined time [selecting a particular cell – normal or redundant] earlier than a second predetermined time [outputting a selected data in a selected normal or redundant cell] when the output data from the memory access is expected to be ready at the output data bus; a redundant memory circuit [16] receiving the memory address and the timing signal, and providing output data when the memory address corresponds to a stored memory address in the redundant memory circuit, the output data being provided at the first predetermined time, in accordance with the timing signal; and a selection circuit [15] selecting, for output at the second predetermined time on the data output bus, between the output data of the memory array and the output data of the redundant memory circuit. In columns 15 and 16, Tsang indicated that if a normal cell is defective, a replacement redundant cell would be substituted for that particular cell and its output would be directed to the selection circuit.

With respect to claim 7, Tsang discloses, in figure 1, that there exists a redundant memory [16]. It is noted that an array consists of a plurality of cells, which can be interpreted as being a plurality of sub-arrays of cells.

With respect to claim 9, Tsang discloses, in figure 1, that there exists a memory array [18] having a plurality of memory cells. The cells data when outputted flows to there respective output terminals. The flow of the data output from a particular cell to the output terminal is being interpreted as being pipelined oriented.

5. Claims 10, 16, and 18 are rejected under 35 U.S.C 102(b) as being anticipated by Tsang [U.S. Patent #4,376,300].

With respect to claim 10, Tsang discloses a method comprising: receiving into a memory array [18 via 22] a memory address for performing an access a memory block [it is interpreted that a memory array has a plurality of sub-arrays or blocks] within the memory array corresponding to the memory address; generating [columns 5 and 6 state that there exist timing signals within the memory arrays; hence, it is reasonable to infer that there exist an element to handle the timing signals within the arrays], from the array, a timing signal that is asserted at a first predetermined time [selecting a particular cell – normal or redundant] earlier than a second predetermined time [outputting a selected data in a selected normal or redundant cell] when the output data from the memory access is expected to be ready at an output data bus [26]; receiving into a redundant memory circuit [16] the memory address and the timing signal; providing [via 15] from the redundant memory circuit output data when the memory address

corresponds to a stored memory address in the redundant memory circuit, the output data being provided at the first predetermined time in accordance with the timing signal; and at the second predetermined time, selecting between the output data of the memory array and the output data of the redundant memory circuit for output on the data output bus.

With respect to claim 16, Tsang discloses, in figure 1, that there exists a redundant memory [16]. It is noted that an array consists of a plurality of cells, which can be interpreted as being a plurality of sub-arrays of cells.

With respect to claim 18, Tsang discloses, in figure 1, that there exists a memory array [18] having a plurality of memory cells. The cells data when outputted flows to there respective output terminals. The flow of the data output from a particular cell to the output terminal is being interpreted as being pipelined oriented.

Allowable Subject Matter

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- The memory array provides a second timing signal which is asserted to indicate the second predetermined time.
- The redundant memory circuit comprises a first-in-first-out memory that holds the output data of the redundant memory circuit.

- The redundant memory circuit comprises address comparators.
- Generating, from the memory array, a second timing signal indicating that the output data of the memory array is ready.
- The redundant memory circuit holds the output data of the redundant memory circuit in a first-in-first-out memory.

Conclusion

7. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

9. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
June 17, 2005

MICHAEL TRAN
PRIMARY EXAMINER